

Fig.1 (Prior Art)

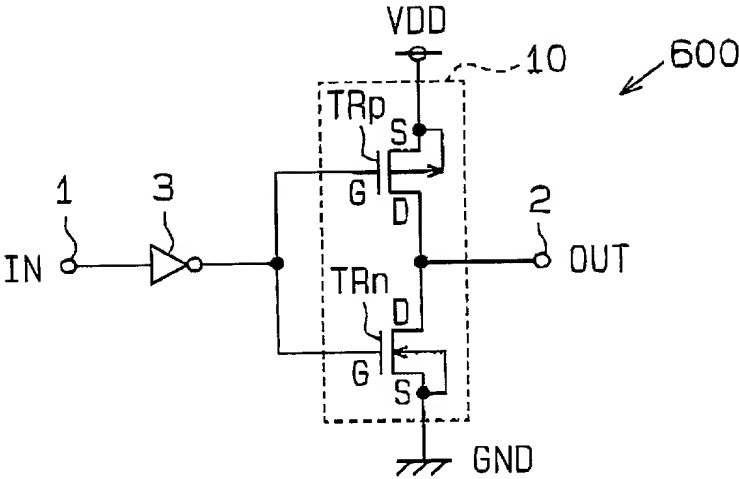
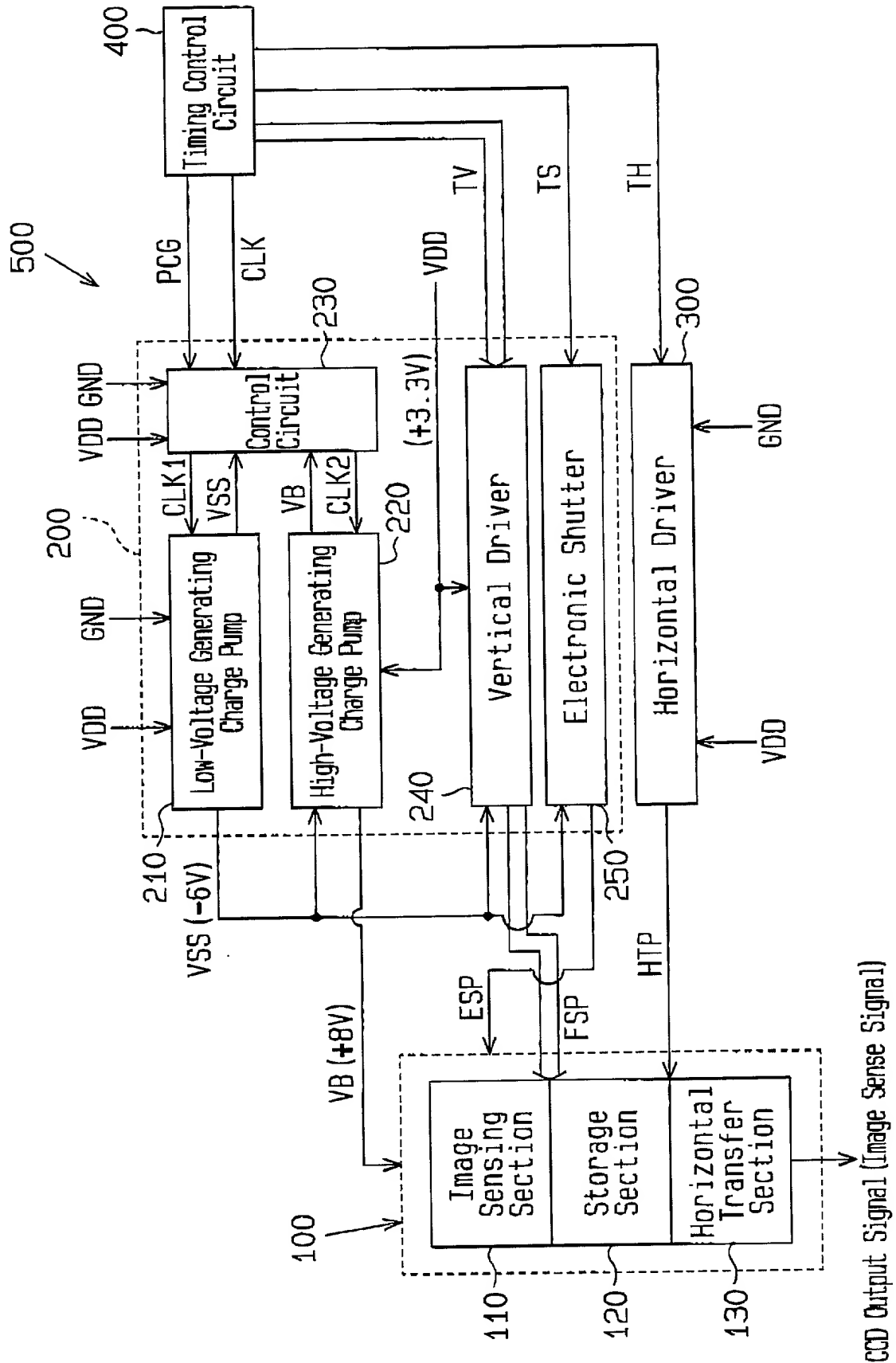


Fig. 2



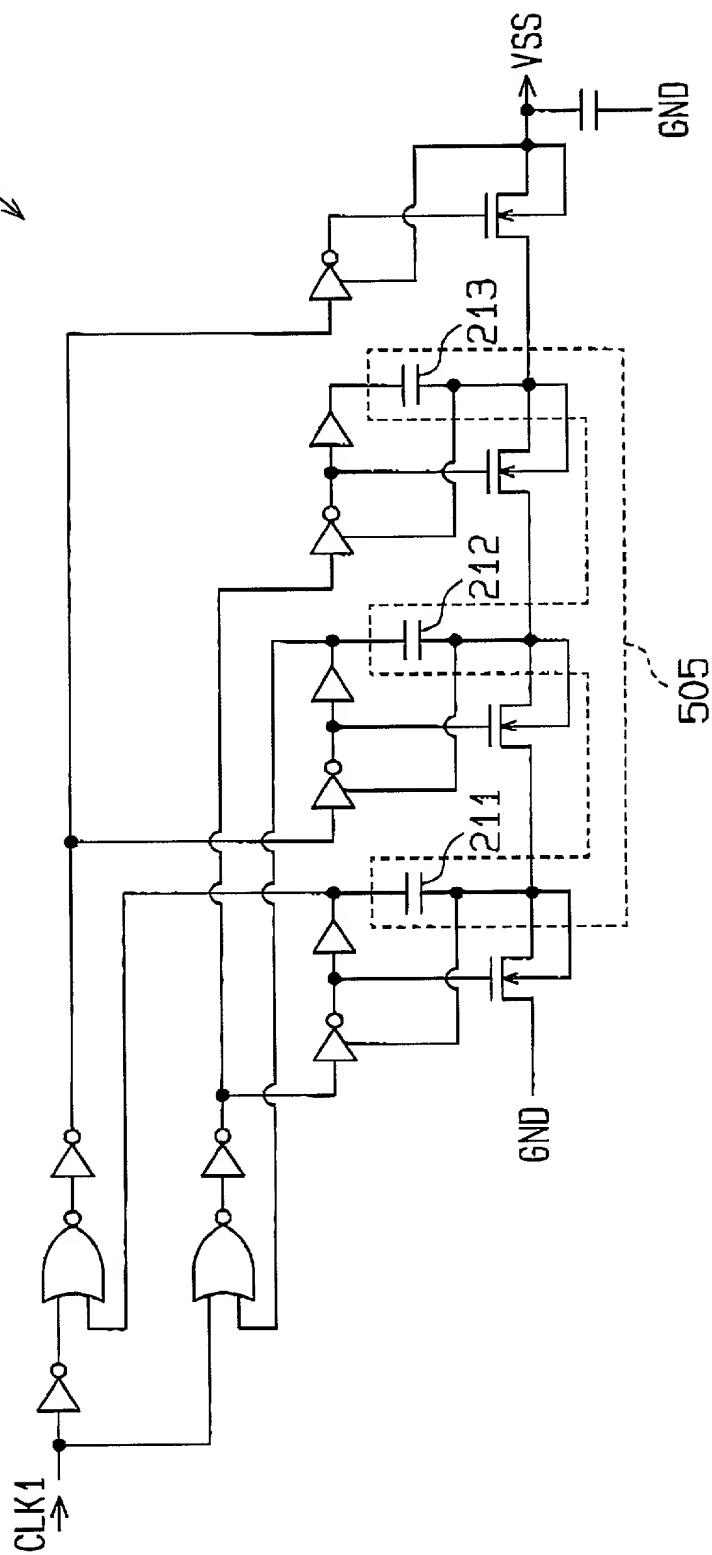


Fig.3

Fig.4(a) Image Sense Signal

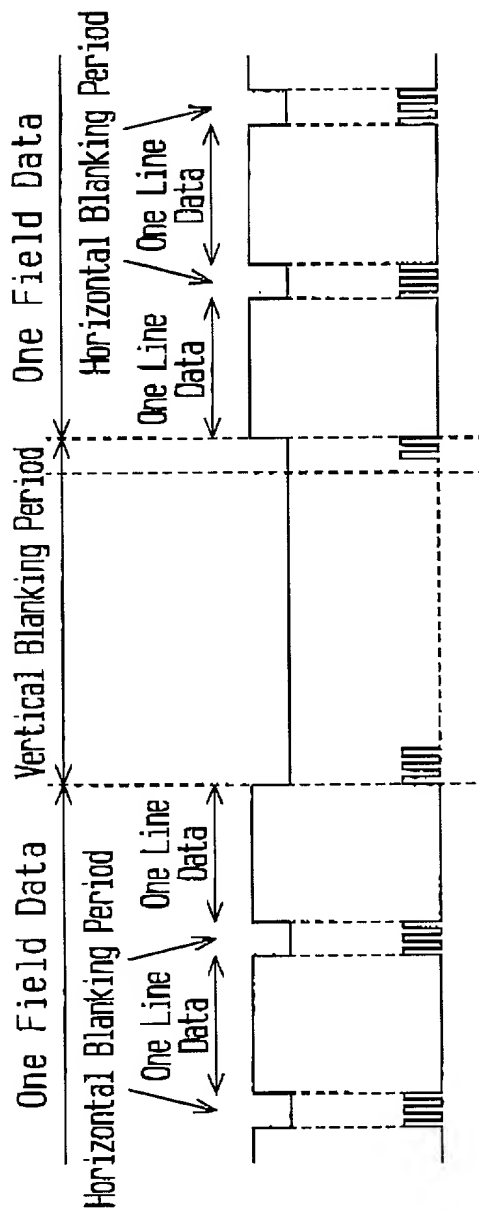


Fig.4(b) Boost Clock Signal CLK1

Fig.4(c) Precharge Instruction Signal POG

Fig.4(d) Frame Shift Pulse Signal FSP

Fig.4(e) VSS

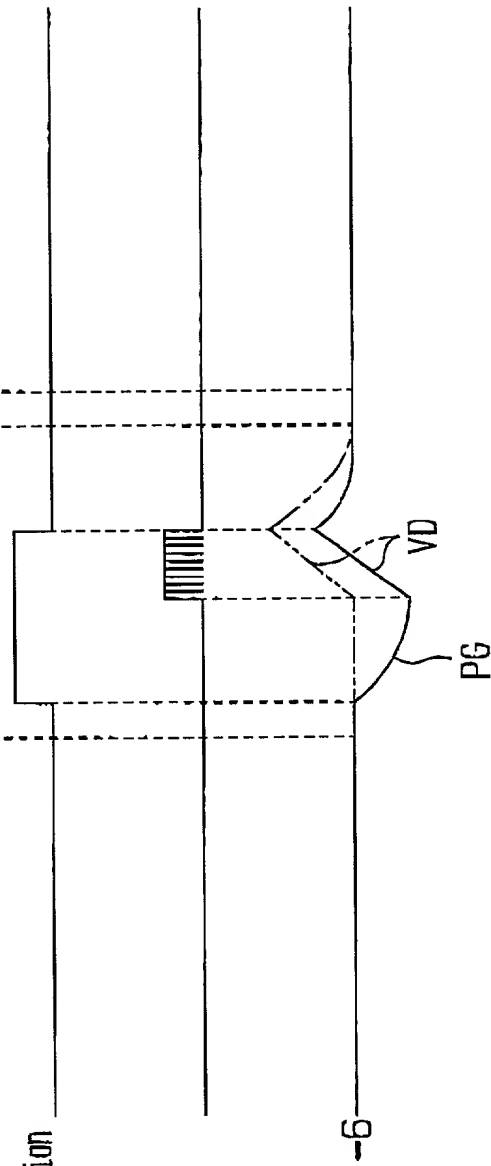


Fig.5

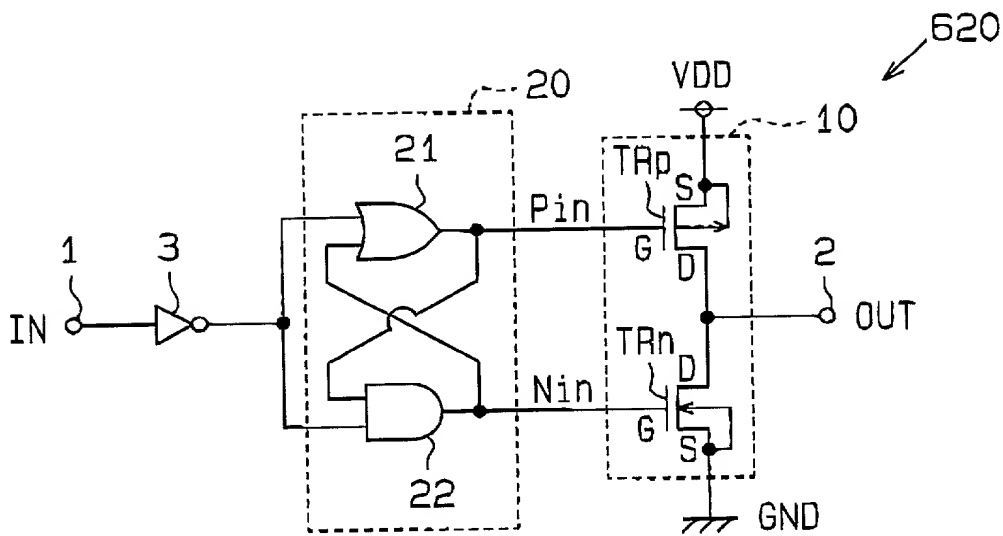


Fig.6 (a) IN $\begin{matrix} H (VDD) \\ L (0) \end{matrix}$

Fig.6 (b) Pin

Fig.6 (c) Nin

Fig.6 (d) OUT

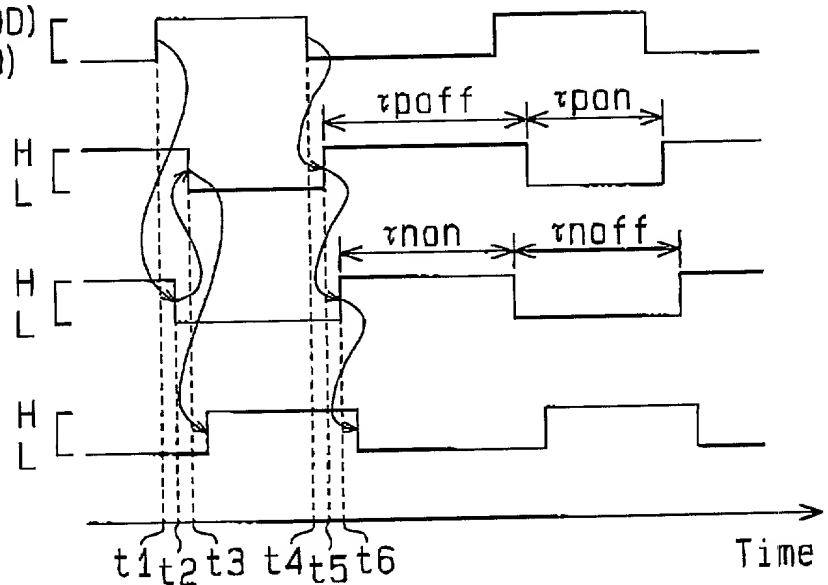


Fig.7

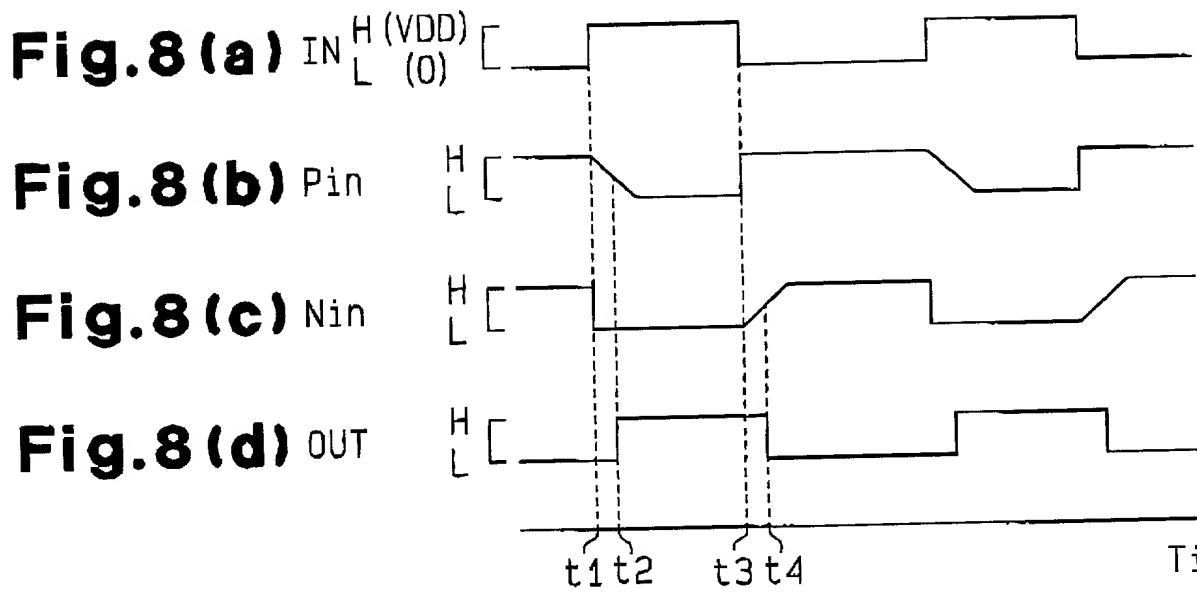
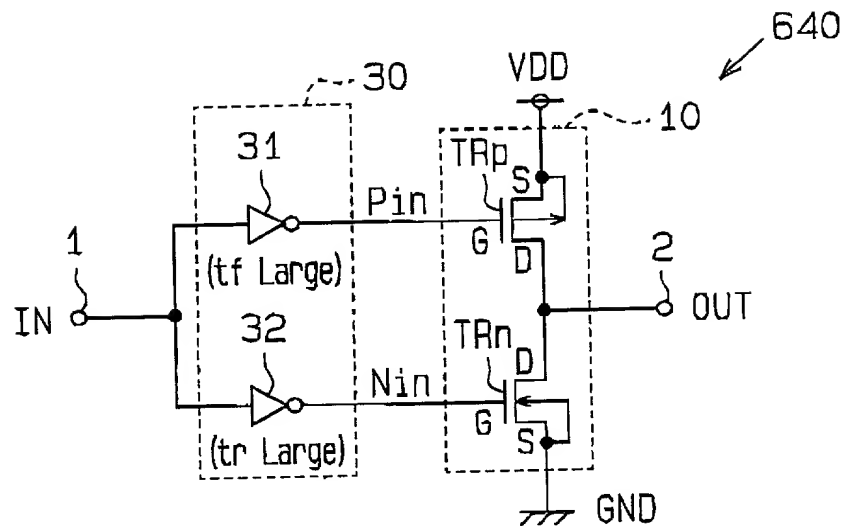


Fig.9

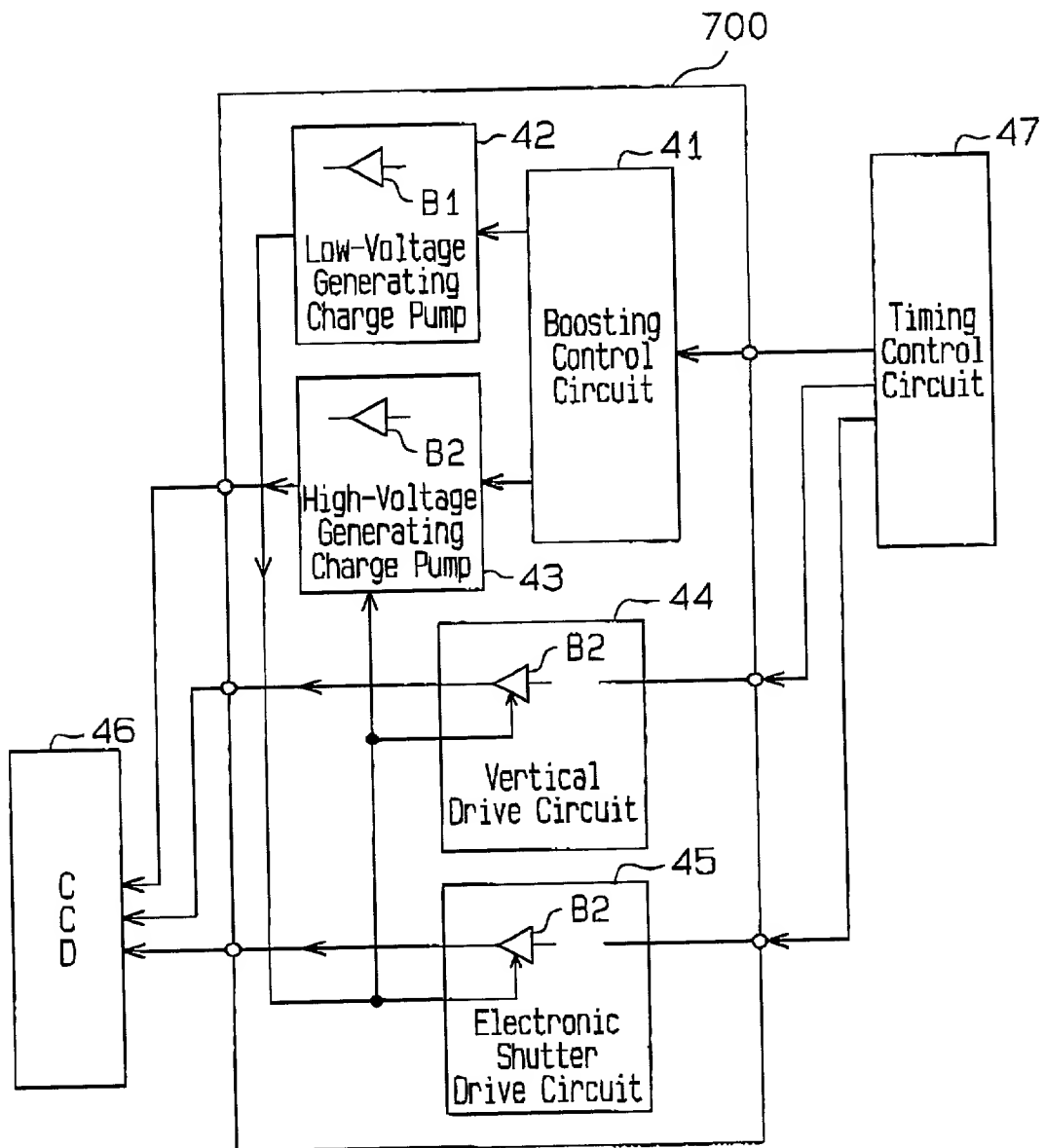


Fig.10

